TABLE 8 — CPU INSTRUCTION MAP

OP	MNEM	MODE	~	#	OP	MNEM	MODE	~	#	OP	MNEM	MODE	~	#	OP	MNEM	MODE	~	#
00	*				34	DES	INHER	3	1	68	ASL	INDXD	6	2	9C	CPX	DIR	5	2
01	NOP	INHER	2	1	35	TXS		3	1	69	ROL		6	2	9D	JSR		5	2
02	*				36	PSHA		3	1	6A	DEC		6	2	9E	LDS		4	2
03	*				37	PSHB		3	1	6B	*				9F	STS	DIR	4	2
04	LSRD		3	1	38	PULX		5	1	6C	INC		6	2	A0	SUBA	INDXD	4	2
05	ASLD		3	1	39	RTS		5	1	6D	TST		6	2	A1	CMPA		4	2
06	TAP		2	1	3A	ABX		3	1	6E	JMP		3	2	A2	SBCA		4	2
07	TPA		2	1	3B	RTI		10	1	6F	CLR	INDXD	6	2	A3	SUBD		6	2
08	INX		3	1	3C	PSHX		4	1	70	NEG	EXTND	6	3	A4	ANDA		4	2
09	DEX		3	1	3D	MUL		10	1	71	*				A5	BITA		4	2
0A	CLV		2	1	3E	WAI		9	1	72	*				A6	LDAA		4	2
0B	SEV		2	1	3F	SWI		12	1	73	COM		6	3	A7	STAA		4	2
0C	CLC		2	1	40	NEGA		2	1	74	LSR		6	3	A8	EORA		4	2
0D	SEC		2	1	41	*				75	*				A9	ADCA		4	2
0E	CLI		2	1	42	*				76	ROR		6	3	AA	ORAA		4	2
0F	SEI		2	1	43	COMA		2	1	77	ASR		6	3	AB	ADDA		4	2
10	SBA		2	1	44	LSRA		2	1	78	ASL		6	3	AC	CPX		6	2
11	CBA		2	1	45	*				79	ROL		6	3	AD	JSR		6	2
12	*				46	RORA		2	1	7A	DEC		6	3	AE	LDS		5	2
13	*				47	ASRA		2	1	7B	*				AF	STS	INDXD	5	2
14	*				48	ASLA		2	1	7C	INC		6	3	B0	SUBA	EXTND	4	3
15	*				49	ROLA		2	1	7D	TST		6	3	B1	CMPA		4	3
16	TAB		2	1	4A	DECA		2	1	7E	JMP		3	3	B2	SBCA		4	3
17	TBA		2	1	4B	*				7F	CLR	EXTND	6	3	B3	SUBD		6	3
18	*				4C	INCA		2	1	80	SUBA	IMMED	2	2	B4	ANDA		4	3
19	DAA	INHER	2	1	4D	TSTA		2	1	81	CMPA		2	2	B5	BITA		4	3
1A	*				4E	*				82	SBCA		2	2	B6	LDAA		4	3
1B	ABA	INHER	2	1	4F	CLRA		2	1	83	SUBD		4	3	B7	STAA		4	3
1C	*				50	NEGB		2	1	84	ANDA		2	2	B8	EORA		4	3
1D	*				51	*				85	BITA		2	2	B9	ADCA		4	3
1E	*				52	*				86	LDAA		2	2	BA	ORAA		4	3
1F	*				53	COMB		2	1	87	*				BB	ADDA		4	3
20	BRA	REL	3	2	54	LSRB		2	1	88	EORA		2	2	BC	CPX		6	3
21	BRN		3	2	55	*				89	ADCA		2	2	BD	JSR		6	3
22	BHI		3	2	56	RORB		2	1	8A	ORAA		2	2	BE	LDS		5	3
23	BLS		3	2	57	ASRB		2	1	8B	ADDA		2	2	BF	STS	EXTND	5	3
24	BCC		3	2	58	ASLB		2	1	8C	CPX	IMMED	4	3	C0	SUBB	IMMED	2	2
25	BCS		3	2	59	ROLB		2	1	8D	BSR	REL	6	2	C1	CMPB		2	2
26	BNE		3	2	5A	DECB		2	1	8E	LDS	IMMED	3	3	C2	SBCB		2	2
27	BEQ		3	2	5B	*				8F	*				C3	ADDD		4	3
28	BVC		3	2	5C	INCB		2	1	90	SUBA	DIR	3	2	C4	ANDB		2	2
29	BVS		3	2	5D	TSTB		2	1	91	CMPA		3	2	C5	BITB		2	2
2A	BPL		3	2	5E	*				92	SBCA		3	2	C6	LDAB		2	2
2B	BMI		3	2	5F	CLRB	INHER	2	1	93	SUBD		5	2	C7	*			
2C	BGE		3	2	60	NEG	INDXD	6	2	94	ANDA		3	2	C8	EORB		2	2
2D	BLT		3	2	61	*				95	BITA		3	2	C9	ADCB		2	2
2E	BGT		3	2	62	*				96	LDAA		3	2	CA	ORAB		2	2
2F	BLE	REL	3	2	63	COM		6	2	97	STAA		3	2	CB	ADDB		2	2
30	TSX	INHER	3	1	64	LSR		6	2	98	EORA		3	2	CC	LDD		3	3
31	INS		3	1	65	*				99	ADCA		3	2	CD	*			
32	PULA		4	1	66	ROR		6	2	9A	ORAA		3	2	CE	LDX	IMMED	3	3
33	PULB		4	1	67	ASR	INDXD	6	2	9B	ADDA		3	2	CF	*			

OP	MNEM	MODE	~	#
D0	SUBB	DIR	3	2
D1	CMPB		3	2
D2	SBCB		3	2
D3	ADDD		5	2
D4	ANDB		3	2
D5	BITB		3	2
D6	LDAB		3	2
D7	STAB		3	2
D8	EORB		3	2
D9	ADCB		3	2
DA	ORAB		3	2
DB	ADDB		3	2
DC	LDD		4	2
DD	STD		4	2
DE	LDX		4	2
DF	STX	DIR	4	2
E0	SUBB	INDXD	4	2
E1	CMPB		4	2
E2	SBCB		4	2
E3	ADDD		6	2
E4	ANDB		4	2
E5	BITB		4	2
E6	LDAB		4	2
E7	STAB		4	2
E8	EORB		4	2
E9	ADCB		4	2
EA	ORAB		4	2
EB	ADDB		4	2
EC	LDD		5	2
ED	STD		5	2
EE	LDX		5	2
EF	STX	INDXD	5	2
F0	SUBB	EXTND	4	3
F1	CMPB		4	3
F2	SBCB		4	3
F3	ADDD		6	3
F4	ANDB		4	3
F5	BITB		4	3
F6	LDAB		4	3
F7	STAB		4	3
F8	EORB		4	3
F9	ADCB		4	3
FA	ORAB		4	3
FB	ADDB		4	3
FC	LDD		5	3
FD	STD		5	3
FE	LDX		5	3
FF	STX	EXTND	5	3

*UNDEFINED OP CODE

NOTES:

1. Addressing Modes
   INHER ≡ Inherent INDXD ≡ Indexed IMMED ≡ Immediate
   REL ≡ Relative EXTND ≡ Extended DIR ≡ Direct
2. Unassigned opcodes are indicated by "*" and should not be executed.
3. Codes marked by "T" force the PC to function as a 16-bit counter.

CONDITION CODE REGISTER — The condition code register indicates the results of an instruction and includes the following five condition bits: negative (N), zero (Z), overflow (V), carry/borrow from MSB (C), and half carry from bit 3 (H). These bits are testable by the conditional branch instructions. Bit 4 is the interrupt mask (I bit) and inhibits all maskable interrupts when set. The two unused bits, B6 and B7, are read as ones.

ADDRESSING MODES

Six addressing modes can be used to reference memory. A summary of the addressing modes for all instructions is presented in Tables 9 through 12, where execution times are provided in E cycles. Instruction execution times are summarized in Table 13. With an input frequency of 4 megahertz, one E cycle is equivalent to one microsecond. A description of selected instructions is shown in Figure 21.

IMMEDIATE ADDRESSING — The operand or immediate byte(s) is contained in the following byte(s) of the instruction where the number of bytes matches the size of the register. These are two or three byte instructions.

DIRECT ADDRESSING — The least significant byte of the operand address is contained in the second byte of the instruction and the most significant byte is assumed to be $00. Direct addressing allows the user to access $00 through $FF using two byte instructions and execution time is reduced by eliminating the additional memory access. In most applications, the 256-byte area is reserved for frequently referenced data.

EXTENDED ADDRESSING — The second and third bytes of the instruction contain the absolute address of the operand. These are three byte instructions.